Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8040	updat$3 near3 (lsb or bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 10:10
L2	16723	updat$3 near3 register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 10:10
L3	65	(l1 or l2) with asynchronous	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 10:13
L4	640	gulick.inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 10:13
L5	4	l3 and l4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 10:42
L6	5	l3 same (performance adj2 register)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 10:43
L7	2	("09852372" or "09852942" or "09853395" or "09853446" or "09870447" or "09870889" or "09853225" or "09871084" or "09871511" or "09544858" or "09853226" or "09853465" or "09853443" or "09853437" or "09853335" or "09853234" or "09870890")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 11:11
L8	2	"5923756".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 11:12

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	261	("$6random number generator" or prng)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:20
L2	0	l1 same ((performance or entropy) adj2 register)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:21
L3	0	l1 and ((performance or entropy) adj2 register)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:21
L4	0	l1 same (updat$3 near3 (lsb or bit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:22
L5	8	l1 and (updat$3 near3 (lsb or bit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:22

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	23747	generat$3 near3 ("random number")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:27
L2	7988	updat$3 near3 ("least significant bit" or bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:28
L3	1479	performance adj3 register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:29
L4	6	l1 same l3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:29
L5	52	l1 same l2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:35
L6	0	l5 same asynchronous$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:35
L7	9	l5 and asynchronous$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 12:36

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1 Track 7: compilers and operating systems: Dynamic run-time architecture techniques for enabling continuous optimization

Tipp Moseley, Alex Shye, Vijay Janapa Reddi, Matthew Iyer, Dan Fay, David Hodgdon, Joshua L. Kihm, Alex Settle, Dirk Grunwald, Daniel A. Connors

May 2005 **Proceedings of the 2nd conference on Computing frontiers**

Full text available: pdf(331.25 KB) Additional Information: full citation, abstract, references, index terms

Future computer systems will integrate tens of multithreaded processor cores on a single chip die, resulting in hundreds of concurrent program threads sharing system resources. These designs will be the cornerstone of improving throughput in high-performance computing and server environments. However, to date, appropriate systems software (operating system, run-time system, and compiler) technologies for these emerging machines have not been adequately explored. Future processors will require so ...

Keywords: multithreading, performance counters, profiling, scheduling

2 Predicting the impact of optimizations for embedded systems

Min Zhao, Bruce Childers, Mary Lou Soffa

June 2003 **ACM SIGPLAN Notices , Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems**, Volume 38 Issue 7

Full text available: pdf(281.53 KB) Additional Information: full citation, abstract, references, citings, index terms

When applying optimizations, a number of decisions are made using fixed strategies, such as always applying an optimization if it is applicable, applying optimizations in a fixed order and assuming a fixed configuration for optimizations such as tile size and loop unrolling factor. While it is widely recognized that these fixed strategies may not be the most appropriate for producing high quality code, especially for embedded systems, there are no general and automatic strategies that do otherwi ...

Keywords: code models, embedded systems, loop optimizations, optimization models, optimizing compilers, prediction, resource models

3 Exploiting parallel microprocessor microarchitectures with a compiler code generator

W. W. Hwu, P. P. Chang

May 1988 **ACM SIGARCH Computer Architecture News , Proceedings of the 15th Annual International Symposium on Computer architecture**, Volume 16 Issue 2

Full text available: pdf(890.51 KB) Additional Information: full citation, abstract, references, citings, index terms

With advances in VLSI technology, microprocessor designers can provide more microarchitectural parallelism to increase performance. We have identified four major forms of such parallelism: multiple microoperations issued per cycle, multiple result distribution buses, multiple execution units, and pipelined execution units. The experiments reported in this paper address two important issues: The effects of these forms and the appropriate balance among them. A central microar ...

4 RS-FDRA: a register sensitive software pipelining algorithm for embedded VLIW processors

Cagdas Akturan, Margarida F. Jacome

April 2001 **Proceedings of the ninth international symposium on Hardware/software codesign**

Full text available: pdf(848.80 KB) Additional Information: full citation, abstract, references, citings, index terms

The paper proposes a novel software-pipelining algorithm, *Register Sensitive Force Directed Retiming Algorithm (RS-FDRA)*, suitable for optimizing compilers targeting embedded VLIW processors. The key difference between RS-FDRA and previous approaches is that our algorithm can handle *code size constraints* along with latency and resource constraints. This capability enables the exploration of pareto "optimal" points with respect to *code size* and *performance*

***Keywords**: VLIW processors, embedded systems, optimizing compilers, retiming, software pipelining*

5 BPF+: exploiting global data-flow optimization in a generalized packet filter architecture

Andrew Begel, Steven McCanne, Susan L. Graham

August 1999 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication**, Volume 29 Issue 4

Full text available: pdf(1.55 MB) Additional Information: full citation, abstract, references, citings, index terms

A *packet filter* is a programmable selection criterion for classifying or selecting packets from a packet stream in a generic, reusable fashion. Previous work on packet filters falls roughly into two categories, namely those efforts that investigate flexible and extensible filter abstractions but sacrifice performance, and those that focus on low-level, optimized filtering representations but sacrifice flexibility. Applications like network monitoring and intrusion detection, however, requ ...

6 The impact of battery capacity and memory bandwidth on CPU speed-setting: a case study

Thomas L. Martin, Daniel P. Siewiorek

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**

Full text available: pdf(717.86 KB) Additional Information: full citation, references, citings, index terms

7 Exploiting software interfaces for performance measurement

Douglas P. Konkin, Gregory M. Oster, Richard B. Bunt

October 1998 **Proceedings of the first international workshop on Software and performance**

Full text available: pdf(1.20 MB) Additional Information: full citation, references, index terms

8 Improving the ratio of memory operations to floating-point operations in loops

Steve Carr, Ken Kennedy

November 1994 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 16 Issue 6

Full text available: pdf(2.49 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Over the past decade, microprocessor design strategies have focused on increasing the computational power on a single chip. Because computations often require more data from cache per floating-point operation than a machine can deliver and because operations are pipelined, idle computational cycles are common when scientific applications are executed. To overcome these bottlenecks, programmers have learned to use a coding style that ensures a better balance between memory references and flo ...

Keywords: balance, unroll-and-jam

9 An analysis of a resource efficient checkpoint architecture

Haitham Akkary, Ravi Rajwar, Srikanth T. Srinivasan

December 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 1 Issue 4

Full text available: pdf(757.69 KB) Additional Information: full citation, abstract, references, index terms

Large instruction window processors achieve high performance by exposing large amounts of instruction level parallelism. However, accessing large hardware structures typically required to buffer and process such instruction window sizes significantly degrade the cycle time. This paper proposes a novel checkpoint processing and recovery (CPR) microarchitecture, and shows how to implement a large instruction window processor without requiring large structures thus permitting a high clock frequency ...

Keywords: Computer architecture, checkpoint architecture, high-performance computing, scalable architecture

10 Retiming with Interconnect and Gate Delay

Chris Chu, Evangeline F. Y. Young, Dennis K. Y. Tong, Sampath Dechu

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(161.83 KB) Additional Information: full citation, abstract, index terms

In this paper, we study the problem of retiming of sequential circuitswith both interconnect and gate delay. Most retiming algorithms haveassumed ideal conditions for the non-logical portions of the datapaths, which are not sufficiently accurate to be used in high performancecircuits today. In our modeling, we assume that the delay ofa wire is directly proportional to its length. This assumption is reasonablesince the quadratic component of a wire delay is significantlysmaller than its linear co ...

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